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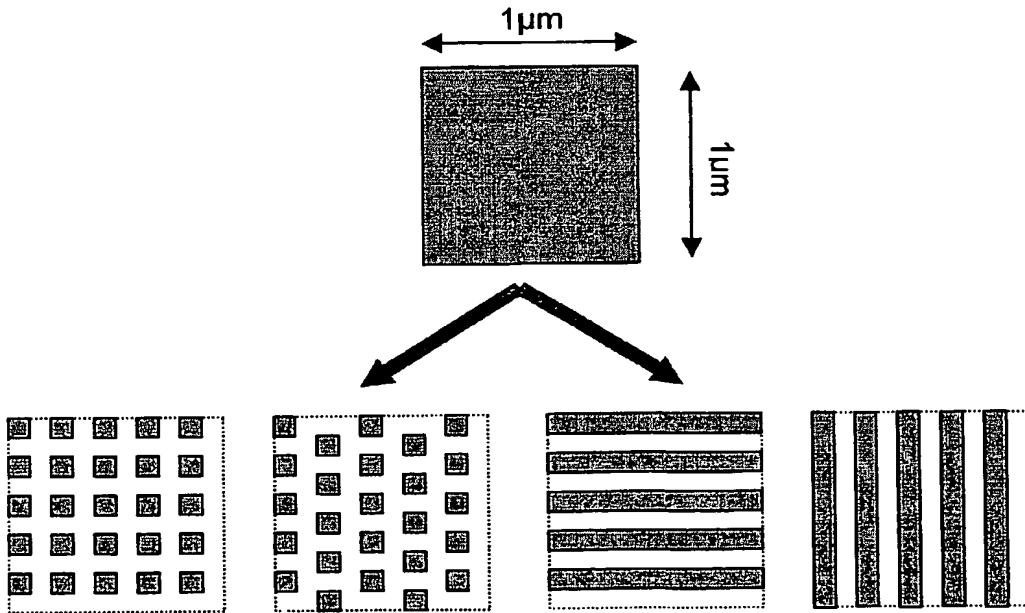
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(54) Title: OVERLAY METROLOGY MARK



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(57) Abstract: An overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure comprising a first mark portion associated with and in particular developed on a first layer and a second mark portion associated with and in particular developed on the surface of a second layer, wherein each mark portion comprises a single two dimensional generally orthogonal array of individual test structures. A method of marking and a method of determining overlay error are also described.



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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/544

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category ^o	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 02/19415 A (KLA TENCOR CORP) 7 March 2002 (2002-03-07) page 1, lines 9-23 page 2, lines 23-26 page 7, lines 1-4 page 11, line 12 - page 12, line 10 page 23, line 4 - page 24, line 7 page 25, line 24 - page 26, line 3 page 30, line 32 - page 32, line 8; figure 8 page 46, line 16 - page 47, line 29; figure 19 page 50, lines 7-20 page 56, line 26 - page 57, line 2 ----- -/-	1-12, 15-22

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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